## PATENT APPLICATION

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Patent Application of

YOSHIKAZU KUROSE

ATTN: APPLICATIONS BRANCH

Serial No. 09/283,231

Filed: April 1, 1999

For: IMAGE PROCESSING APPARATUS )

AND METHOD OF THE SAME

AND METHOD OF THE SAME

## LETTER RE: SUBMISSION OF FORMAL DRAWINGS

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

We have enclosed formal drawings in the above-identified application to replace the informal drawings submitted with the application on April 1, 1999.

Respectfully submitted,

Dated: June 25, 1999

Honald B. Kananen Reg. No. 24,104

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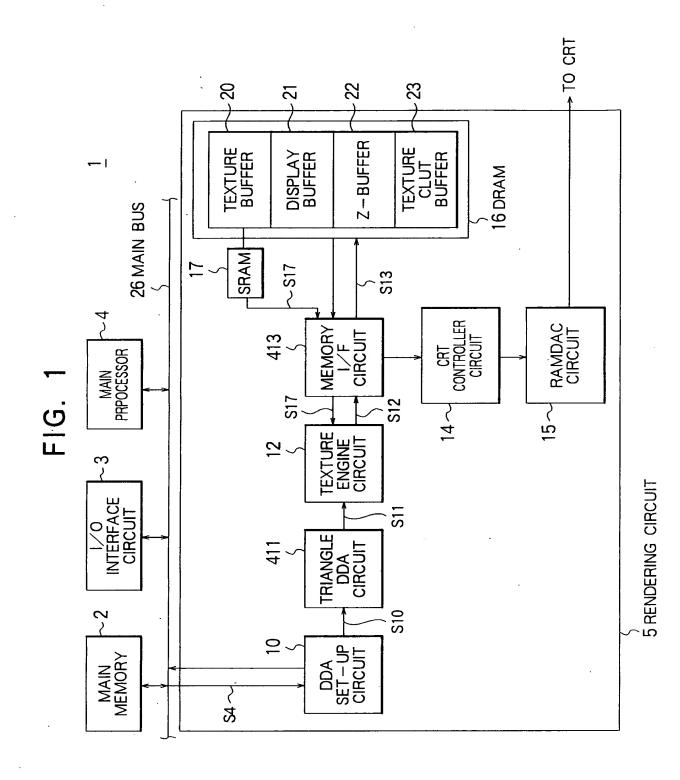


FIG. 2

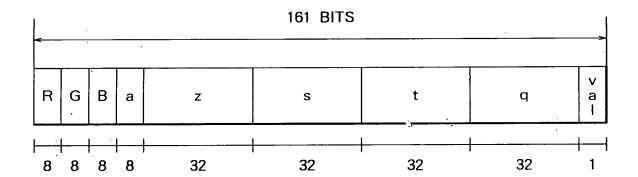
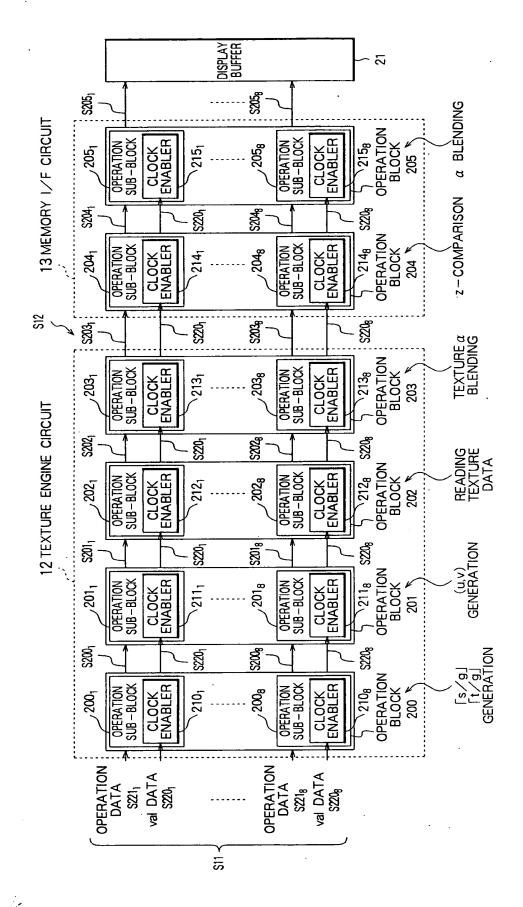


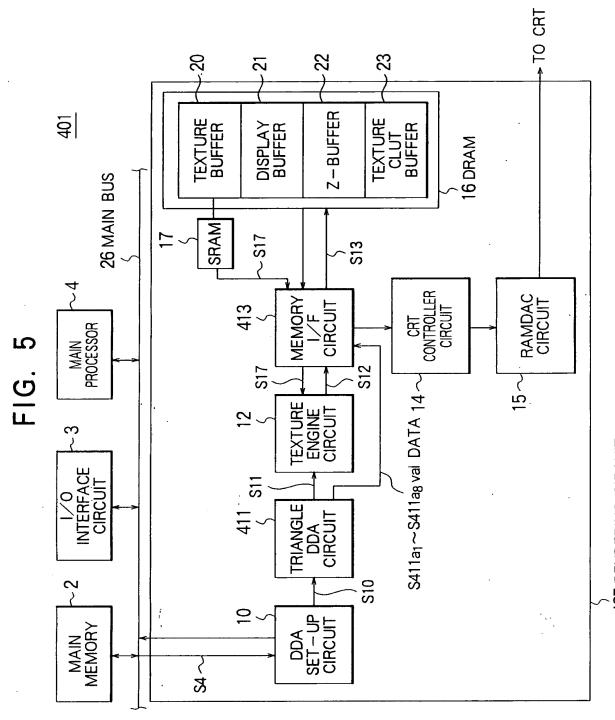
FIG. 3



~ 222 2011 DATA FLIP FLOP (160bit) FLAG FLIP FLOP (1bit) CLOCK 733 띰 522 DATA FLIP FLOP (160bit) FLAG FLIP FLOP (1bit) 224 2001 CLOCK ENABLER S210₁~ val DATA S220<sub>1</sub> – SYSTEM CLOCK S250<sub>1</sub>– OPERATION S2211 DATA

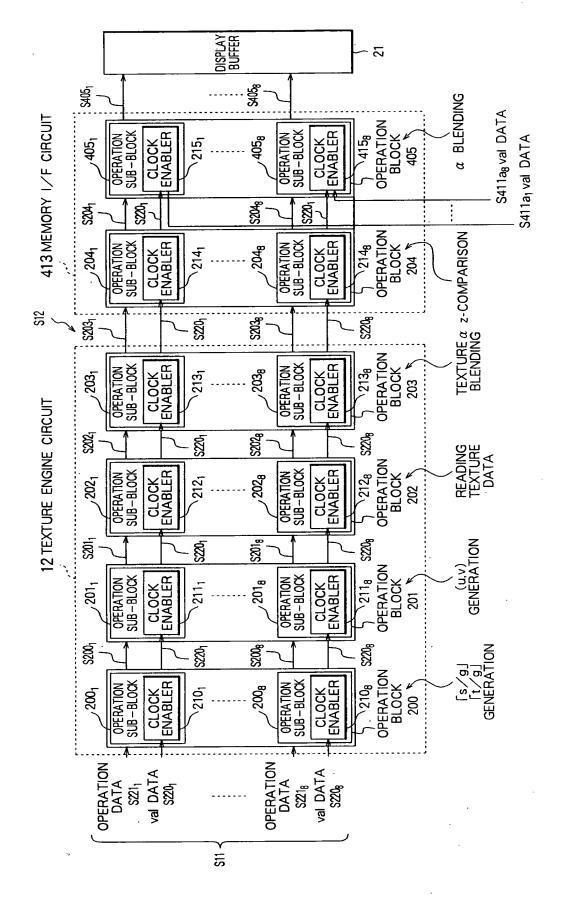
226

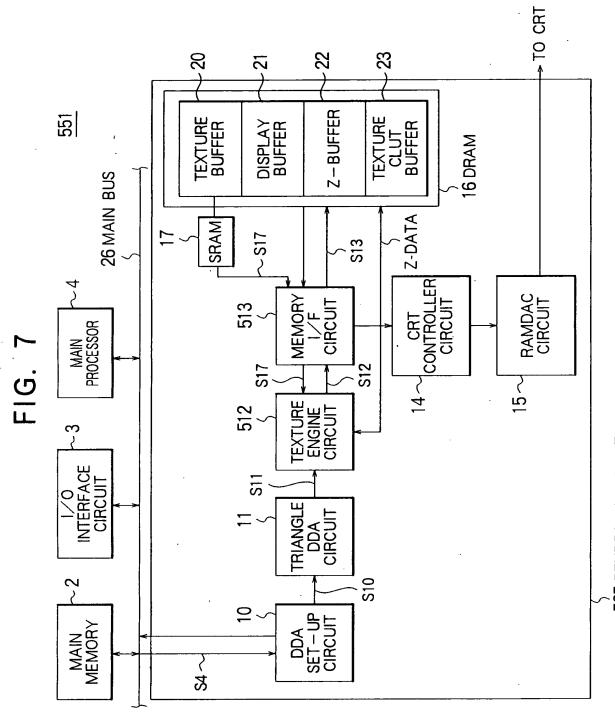
띰



425 RENDERING CIRCUIT

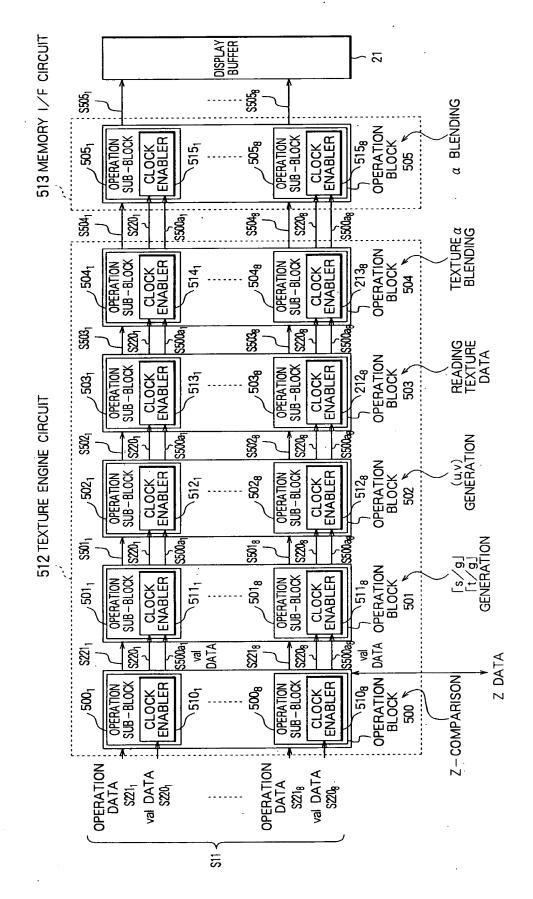
FIG. 6





525 RENDERING CIRCUIT

FIG. 8



8 8 413 MEMORY I/F CIRCUIT CLOCK ENABLER 405, SSA OPERATION SUB-BLOCK CLOCK ENABLER 2041 **S12** . S203, OPERATION SUB – BLOCK CLOCK ENABLER ,203, 12 TEXTURE ENGINE CIRCUIT S202 CLOCK ENABLER ,202, 5201, OPERATION SUB - BLOCK CLOCK ENABLER 201 S200 OPERATION SUB - BLOCK CLOCK ENABLER 200 OPERATION DATA S221,

DISPLAY BUFFER

S400a<sub>1</sub> val DATA

6 5 1

FIG. 10

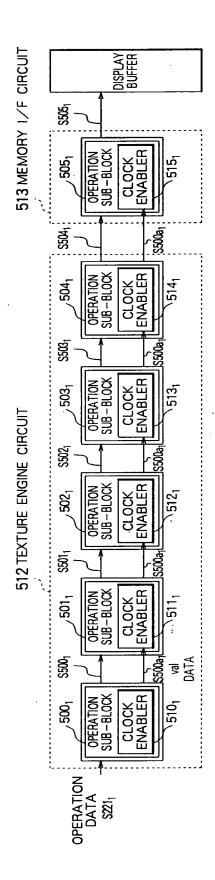


FIG. 11

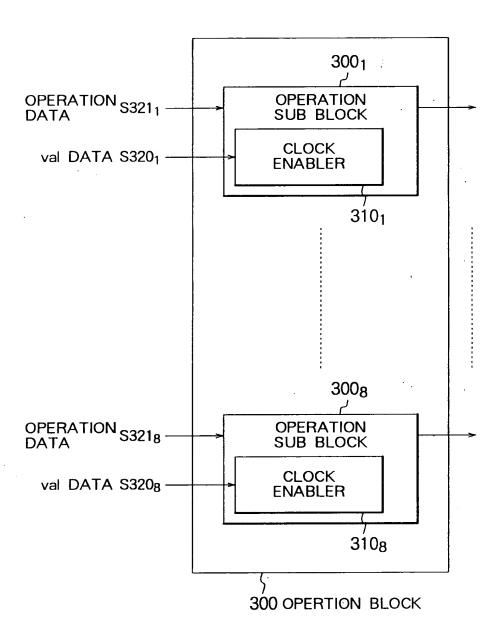


FIG. 12

